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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
BRINEY III, WALTER F	

ART UNIT	PAPER NUMBER
2646	

DATE MAILED: 08/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/091,451	CHANG ET AL.	
	Examiner	Art Unit	
	Walter F. Briney III	2646	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 March 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

1. **Claims 4 and 5 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.**

Claim 4 recites the limitation "the constriction variable resistor" in line 2. There is insufficient antecedent basis for this limitation in the claim. For the purposes of this action, the above cited limitation is being interpreted as "the transistor" in accordance with currently amended claim 1, which renamed "the constriction variable resistor" to "the transistor".

Claim 5 is dependent on claim 4, and is rejected under 35 USC § 112, second paragraph, for the same reasons.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. **Claims 1-11, 14 and 17 are rejected under 35 U.S.C. 102(e) as being anticipated by Jain (US Patent 6,275,088).**

Claim 1 is limited to *an apparatus of ring-back constriction, coupled to a transmission line, for constricting a ring-back effect.* Jain discloses a method and apparatus for dynamic impedance clamping of a digital signal delivered over a transmission line. See Abstract. As seen in figure 5, Jain depicts dynamic clamping circuit that includes a *comparator* (36) for comparing the input (16) with an intrinsic threshold or reference voltage defined by the manufacturing process of the gates (50) and (51), a *termination controller* (elements 38 and 66-78), a *termination variable resistor* (32), a *constriction controller* (elements 40 and 80-98) and a *transistor* (34) including a *gate*, *source* and drain, where the transistors intrinsic operation includes varying its resistance based on the voltage difference between the gate and the source.

Alternatively, the circuit of figure 5 could be characterized such that it includes a *termination controller* (elements 40 and 80-98), *termination variable resistor* (34), *constriction controller* (elements 38 and 66-78) and *transistor* (32). In any case, the constriction signal generated by the constriction controller changes from a first to a second voltage immediately proceeding a change in the line signal from a third voltage to a fourth voltage, the constriction signal then returns to the first voltage after a period defined by either element (40) in the first interpretation provided above or element (38) in the alternative interpretation. Therefore, Jain anticipates all limitations of the claim.

Claim 2 is limited to *the apparatus according to claim 1*, as covered by Jain. In the first interpretation of Jain, *the termination variable resistor* (32) is set at a low resistance when the input signal transitions to a high value, but a subsequent low value

on input line (16) causes the comparator (36) to transition to a low value that immediately forces *resistor* (32) to assume a *high resistance value*. Therefore, Jain anticipates all limitations of the claim.

Claim 3 is limited to *the apparatus according to claim 1*, as covered by Jain. As suggested in the rejection of claim 2, a high to low level transition at the output of comparator (36) causes the resistance of the termination variable resistor to increase. The rate of resistance increase is limited by the intrinsic capacitance exhibited in part by the gate oxide barrier of gate (32) and the driving strength of transistors (70) and (78), thus defining a *transition period*. Therefore, Jain anticipates all limitations of the claim.

Claim 4 is limited to *the apparatus according to claim 1*, as covered by Jain. In the first interpretation of Jain, the *transistor* (34) is at a high value when the input signal is at a steady-state high value as evidenced by the NOR gate (elements 80-94) receiving both a signal and its logical inverse. When the comparator (36) transitions to a low value, the inverted signal is delayed, which causes a positive pulse to momentarily bias transistor (34) into a low resistance state. The resistance of the transistor eventually returns to a high value after a time equal to the propagation through inverter (40). Therefore, Jain anticipates all limitations of the claim.

Claim 5 is limited to *the apparatus according to claim 4*, as covered by Jain. As noted in the rejection of claim 4, the resistance of *transistor* (34) transitions from high to low with the signal level transitioning from high to low, but rising after a delay. Again, the resistance increase is limited by the intrinsic capacitance of transistor (34) and the

driving strength of transistors (82) and (94), these components defining a *transition period*. Therefore, Jain anticipates all limitations of the claim.

Claim 6 is limited to *the apparatus according to claim 1*, as covered by Jain. The *termination controller* of the first interpretation of Jain corresponds to the inverter (38), NAND gate (66) and buffer (elements 68-78). As the term "*weak*" is completely relative, it is fair to suggest that any of transistors (70) and (78) of the buffer correspond to a weak transistor that takes a transition period to change the resistance of the *termination variable resistor* from low value to high value. Therefore, Jain anticipates all limitations of the claim.

Claim 7 is limited to *the apparatus according to claim 6*, as covered by Jain. As shown above in the rejection of claim 6, either transistor (70) or (78), which are responsible for raising the resistance of the *termination variable resistor* (32) can be considered a *weak transistor*. Furthermore, both transistors are *PMOS transistors*. Therefore, Jain anticipates all limitations of the claim.

Claim 8 is limited to *the apparatus according to claim 1*, as covered by Jain. The *constriction controller* of the first interpretation of Jain corresponds to the inverter (40), and NOR gate (elements 80-98). As the term "*weak*" is completely relative, it is fair to suggest that any of transistors (82), (84), (90), (92), (94) and (96) of the NOR gate correspond to a weak transistor that takes a transition period to change the resistance of the *termination variable resistor* from low value to high value. Therefore, Jain anticipates all limitations of the claim.

Claim 9 is limited to *the apparatus according to claim 8*, as covered by Jain. As shown above in the rejection of claim 8, any of transistors (82), (84), (90), (92), (94) and (96), which are responsible for raising the resistance of the *termination variable resistor* (32) can be considered a *weak transistor*. Furthermore, transistors (84) and (90) are *PMOS transistors*. Therefore, Jain anticipates all limitations of the claim.

Claim 10 is limited to *the apparatus according to claim 1*, as covered by Jain. In the first interpretation of Jain, the *termination variable resistor* (32) is clearly a *PMOS transistor*. Therefore, Jain anticipates all limitations of the claim.

Claim 11 is limited to *the apparatus according to claim 1*, as covered by Jain. In the alternative interpretation of Jain, the *transistor* (32) is clearly a *PMOS transistor*. Therefore, Jain anticipates all limitations of the claim.

Claim 14 is limited to *the apparatus according to claim 1*, as covered by Jain. In the second interpretation of Jain, the voltage applied to the source of the *transistor* (32) is clearly higher than that applied to the source of the *termination variable resistor* (34), such that the *constriction voltage* is higher than the *termination voltage*. Therefore, Jain anticipates all limitations of the claim.

Claim 17 is limited to *the apparatus of ring-back constriction, coupled to a transmission line, for constricting a ring-back effect*. As recited, this claim is essentially the same as claim 1, as covered by both Jain and the applicant's admitted prior art in view of Jain. However, this claim is distinguished over claim 1 as it recites that the *constriction controller comprises a delay unit for delaying the comparison signal for a delay period; an inverter for inverting the comparison signal; and a NAND gate for*

receiving the delayed comparison signal and the inverted comparison signal. This new limitation still reads on Jain if interpreted in a third manner. Like in the alternative interpretation of Jain, the *constriction controller* includes a NAND gate (66) that receives two inputs. However, the comparator is considered to be comprised solely of inverter (50) such that inverter (51) produces an inverted comparator signal to the NAND gate. In addition, inverter (54) inverts the inverted comparison signal to effectively regenerate the comparison signal at its output. This regenerated comparison signal is then delayed by inverters (56) and (58) and provided to the second input of NAND gate (66). Therefore, Jain anticipates all limitations of the claim.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 12, 13 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jain.

Claim 12 is limited to *the apparatus according to claim 1*, as covered by Jain. Jain discloses using a 3.3V CMOS process with an undisclosed switching voltage threshold (i.e. *reference voltage*). See column 3, lines 28-37. Therefore, Jain anticipates all limitations of the claim with the exception *wherein the reference voltage is 1 volt.*

In general, certain tradeoffs are made between one voltage level and another, for example: power dissipation, speed, capacitive noise, etc... As such, the CMOS process is a matter of design choice.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use a CMOS process of around 1.5V with an intrinsic switching voltage of 1V instead of the disclosed 3.3V process with an undisclosed switching voltage of Jain since the applicant's disclosure has not specified that a process of 1.5 and a reference voltage of 1V provides any advantage over previously known efforts.

Claim 13 is limited to *the apparatus according to claim 1*, as covered by Jain. For similar reasons presented in the rejection of claim 12, it would have been obvious to fabricate a CMOS system using an operational termination voltage of 1.5V for the first interpretation of Jain.

Claim 15 is limited to *the apparatus according to claim 1*, as covered by Jain. For similar reasons presented in the rejection of claim 12, it would have been obvious to fabricate a CMOS system using an operational constriction voltage in the range of 2.5V to 2.6V for the alternative interpretation of Jain.

4. Claims 1 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over the applicant's admitted prior art (figure 2) in view of Jain.

Claim 1 is limited to *an apparatus of ring-back constriction, coupled to a transmission line, for constricting a ring-back effect.* Applicant's admitted prior art, shown in figure 2, includes a receiving *comparator* (203), which compares a received logic signal from *transmission line* (L) to a reference signal V_{ref}. The output is fed

directly to *a termination controller* (202), which adjusts the resistance of *a variable terminating resistor* (R_t). The net effect is to provide temporary impedance matching. However, no reference to a constriction controller is made in this admitted prior art. Therefore, the applicant's admitted prior art of figure 2 anticipates all limitations of the claim with the exception of *a constriction controller* and *transistor.*

Jain discloses a method and apparatus for dynamic impedance clamping of a digital signal delivered over a transmission line. See Abstract. In particular, the device reduces both the effects of overshoot and undershoot apparent in switching logic states between high and low levels. Figure 6 depicts the dynamic clamping circuit (22) of the invention combined with a prior art ringing clamping circuit (600) that essentially corresponds to the termination resistor (figure 2, element R_t) of the applicant's admitted prior art. In particular, inverter (620) corresponds to the *termination controller* and inverter (630 and 640) is the *termination resistor.* As is known in the art (see Takeda - column 2, line 57, through column 3, line 14), simply using the terminal controller and resistor of the applicant's admitted prior art results in large over and undershoots, requiring further clamping. With respect to the current claim language, Jain depicts a *constriction controller* (elements 40 and 80-98) and a *transistor* (34) including a *gate*, *source* and drain, where the transistors intrinsic operation includes varying its resistance based on the voltage difference between the gate and the source. The constriction signal generated by the constriction controller changes from a first to a second voltage immediately proceeding a change in the line signal from a third voltage to a fourth

voltage, the constriction signal then returns to the first voltage after a period defined by element (40).

It would have been obvious to one of ordinary skill in the art to include the dynamic clamping circuit (22) as taught by Jain with the applicant's admitted prior art comprising a comparator and termination controller for the purpose of eliminating the overshoot/undershoot effects that arise due to impedance mismatches within a transmission line termination.

Claim 16 is limited to *the apparatus according to claim 1*, as covered by the applicant's admitted prior art in view of Jain. The applicant's admitted prior art is intended for use with *a GTL+ (Gunning Transistor Logic Plus) bus*, see paragraph 7. Therefore, the applicant's admitted prior art in view of Jain makes obvious all limitations of the claim.

Response to Arguments

Applicant's arguments with respect to claims 1-17 filed 22 March 2005 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Walter F. Briney III whose telephone number is 571-272-7513. The examiner can normally be reached on M-F 8am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sinh Tran can be reached on 571-272-7564. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

WFB
8/3/05

SINH TRAN
SUPERVISORY PATENT EXAMINER